Self-synchronous circuitry.

Discrete electronic circuits are very diverse, but they can all be divided into two classes: synchronous and asynchronous circuits.

Distinctive features of self-synchronous circuits (SS-circuits) are related to the reliability of their functioning. One of the main problems of the operation of digital electronic circuits is the occurrence of errors.

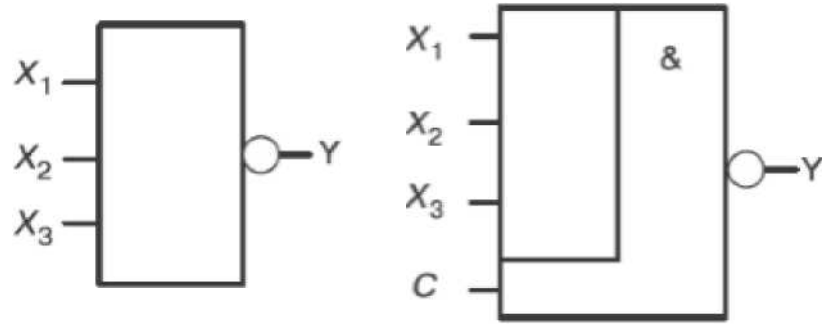
Errors in this case are the inconsistency of the signal values inside the circuit and at its outputs with the correct values. Errors can be caused by external influences and internal reasons.

The internal causes of errors are determined by the way the circuit is constructed and the conditions under which it operates. There are two such reasons:

1. Competition of signals on the elements, that is, such changes in the inputs of the elements that cause false changes in their outputs and, as a result, in the outputs of the entire circuit.

2. The occurrence of circuit failures - occur when the physical performance of internal structures is lost, caused by operating conditions: temperature, power supply voltage, as well as aging of elements and other processes.

Using the example of competitions, you can explain the synchronous and asynchronous principles of operation of circuits (the synchronous principle arose as a way to avoid signal competitions).
Consider the logical element in Fig. a.

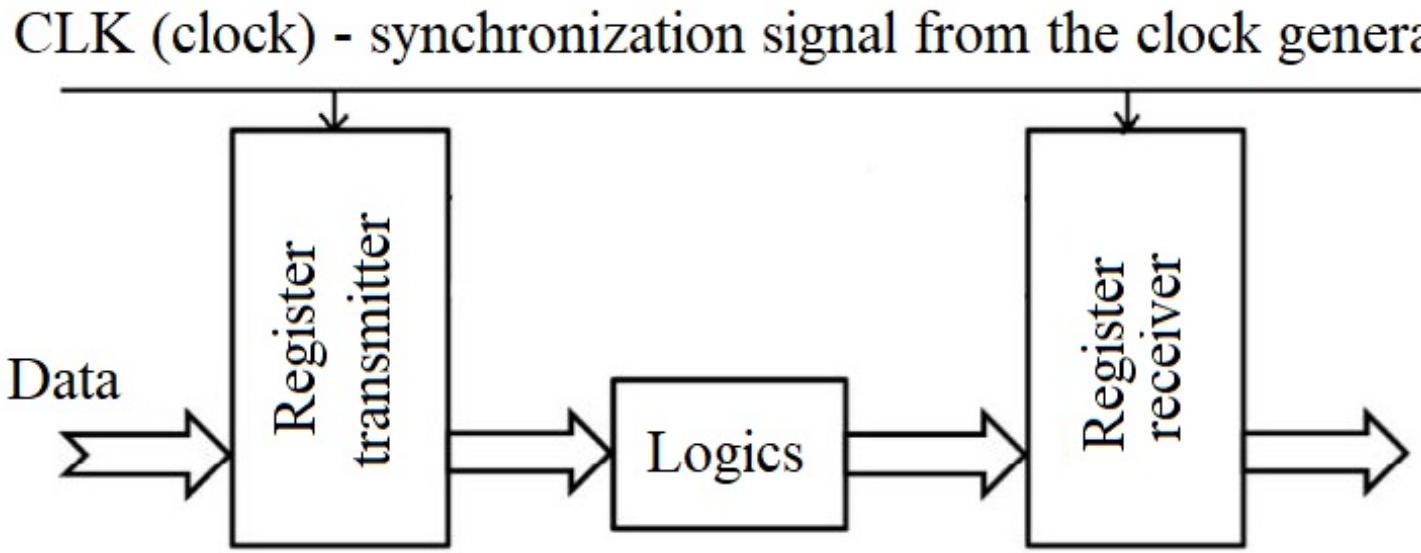


a **b**

Logic element (a) and element with blocking signal C (b)
Since it is impossible to avoid races with an arbitrary order of changes in the input signals of the elements, the only way to combat them will be to order these changes, that is, to introduce signal discipline.
One of the simplest ways of organizing the discipline of signals is the introduction of a blocking signal (Fig. b, signal C).

The second cause of errors is failure of elements.
It is impossible to predict failures during the operation of the circuit, but there will be no errors if the circuit stops immediately after the failure and does not give unpredictable values at the outputs.
This property is called self-checking. However, the standard term that reflects this property is closer to failure resistance, defined as "product properties aimed at maintaining safety in the event of failure."
The uniqueness of SS circuits is that they implement an almost ideal solution: there are no races in them and fault tolerance is ensured, since the circuits are stopped when failures occur.

Synchronous interaction of devices.



The main advantage is the simplicity of device design and minimal equipment costs, which determined the choice of the synchronous principle of circuit construction as the main one in the middle of the 20th century.

Disadvantages of external synchronization:

- the complexity of designing a system for delivering synchronizing signals to synchronization points due to the spread of delays in wires and amplifiers;

- additional power consumption (up to 30-40%);

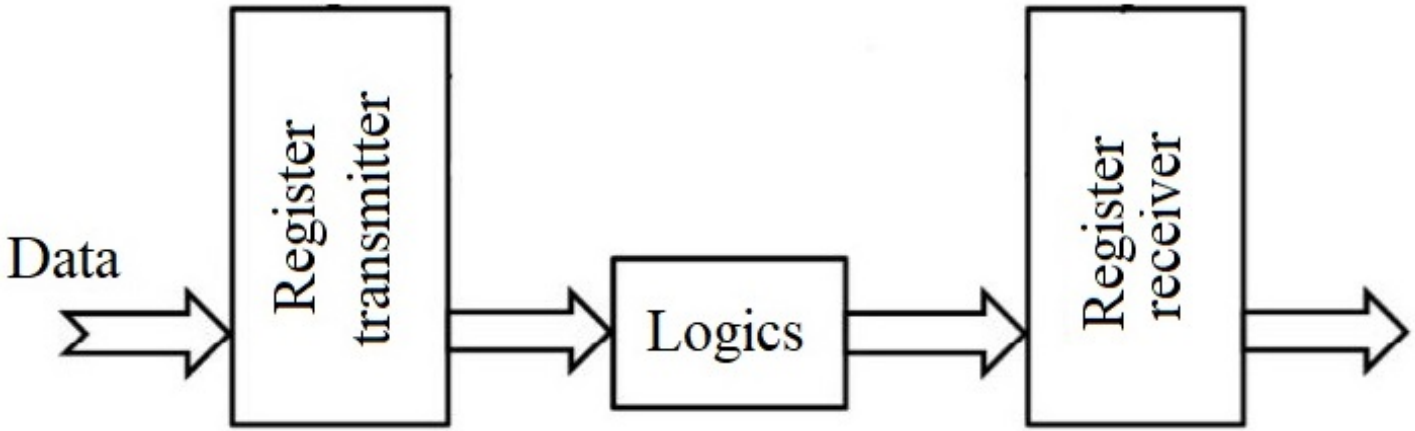
- underutilization of the speed capabilities of the elements (calculation for the "worst case");

- the possibility of parametric failures due to a change in operating conditions;

- a source of interference due to the simultaneous activation of a large number of elements;

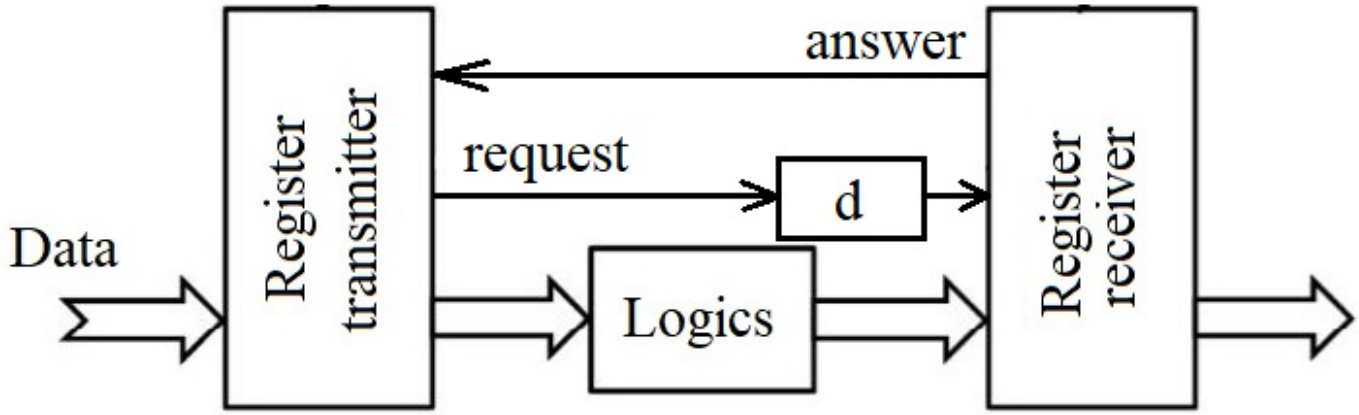
- the difficulty of organizing the coordinated operation of a multiprocessor system with individual synchronization subsystems, because there are no absolutely reliable synchronizers that always have a certain probability of failure. Any such systems are subject to failure.

Classic asynchronous interaction of devices (without the use of "request-response" signals).



The advantage of such devices is the absence of a system for delivering synchronizing signals to synchronization points, however, other disadvantages of synchronous devices remain and additionally new (more complex) problems arise: struggle with logical and functional competitions.

Asynchronous interaction of devices (using request-response signals, using built-in delay).



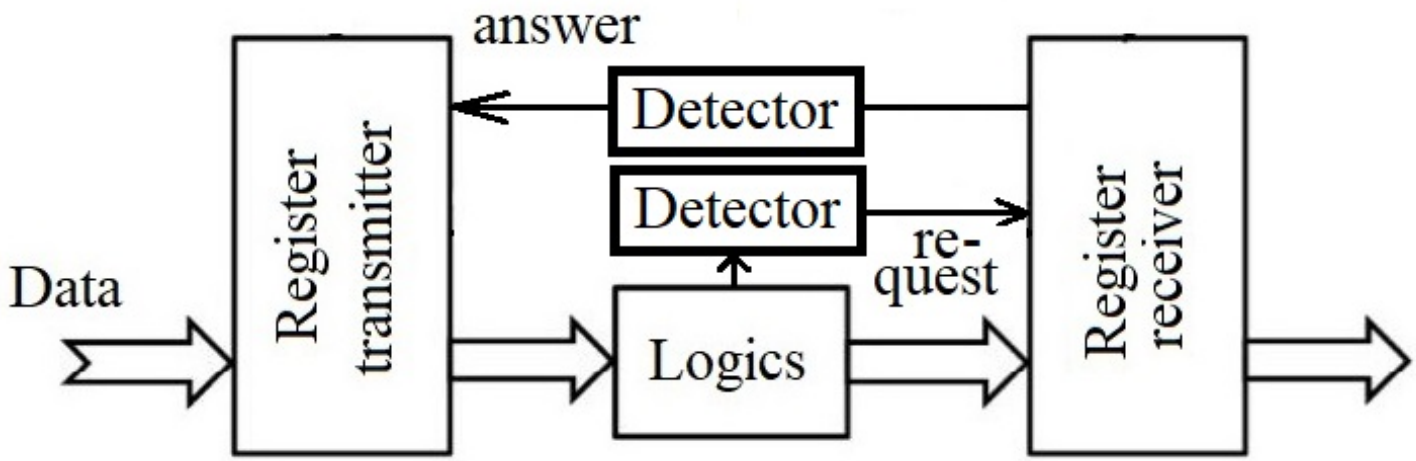
"Request-response" interaction can be implemented using a built-in delay (d) or a transient end detector:

- the value of the built-in delay must exceed the maximum delay of the logic circuit and the delay of writing data into the receiving register (receiving device)

- the amount of delay is selected individually based on the characteristics of a specific receiving device. This allows to increase the total traffic of the system with significantly different speed characteristics of its component devices

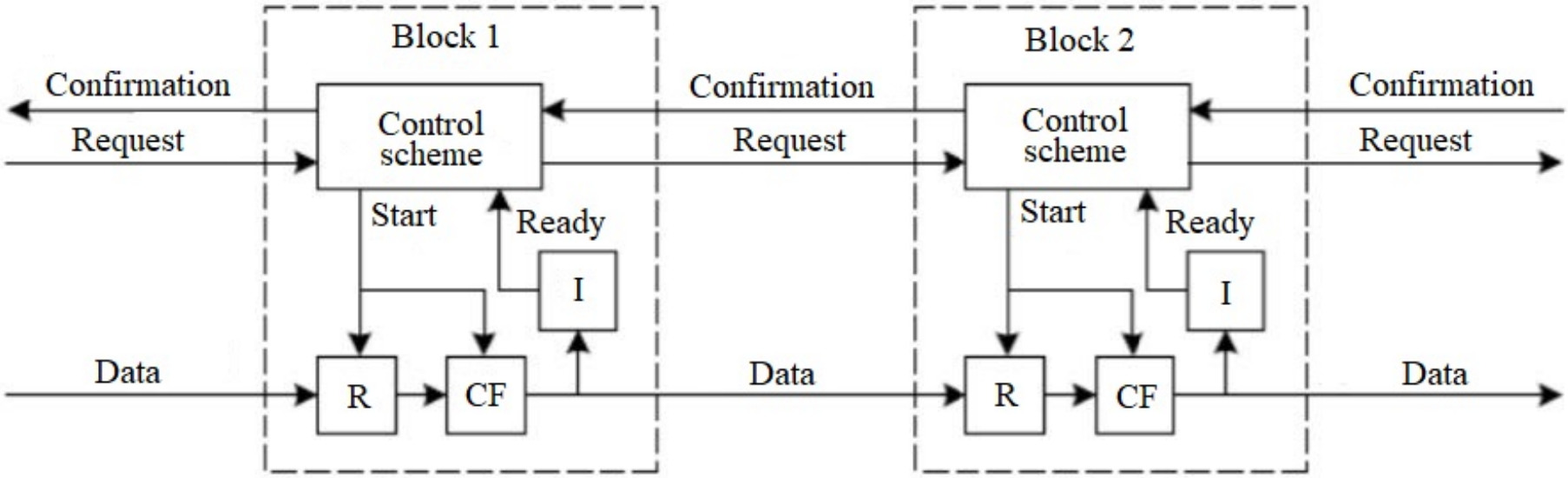
- this structure is very similar to a synchronous implementation: the duration of initiated events is not monitored in any way, and the value of the built-in delay is selected based on the "worst case".

Self-synchronous interaction of devices (use of the detector of the end of transient processes).



- the request detector determines the actual end of transient processes in the logic circuit (the "request" signal is produced);
- the answer determines the actual end of transient processes in the receiver register (the "answer" signal is produced);
- redundant coding of data with self-synchronous codes is used;
- in the event of a failure, the transient process is not completed and the self-synchronizing circuit is stopped.

An example of a SS scheme consisting of two blocks. Each block consists of an asynchronous register (R), which stores data during processing, and a combinational function (CF), which performs data processing. An indicator (I) is connected to the output of the combination function, which monitors the moment when the transition process ends.



The scheme works as follows: data accompanied by the "Request" signal is sent to the input of the block.

If the block is not active at this moment and is ready to receive new data, the control circuit generates a "Start" signal, which writes data into the input register and activates the operation of the combinational function of the block, in addition, a "Confirmation" signal is generated, which shows that the block ready to receive new data.

After some time, upon completion of transient processes, the indicator block generates the "Ready" signal, which shows that the calculations are finished and there are valid data at the output of the block. If a "Confirm" signal arrives from the next block, the control system generates a "Request" signal. The time of block data processing depends on many factors of the operating mode and, specifically, on the processed data.

Potential benefits of CC schemes.

- absence of overhead hardware and energy costs associated with the implementation of an extensive synchronization system:

- maximum speed possible under current operating conditions;

- natural resistance to parametric failures caused by changes in element parameters due to aging processes and adverse environmental influences:

- the maximum possible field of operation (operating capacity range), due only to the physical preservation of the switching properties of the active elements of the basis of implementation and the possibility of working at a reduced supply voltage;

- natural self-checking and self-adjustment in relation to multiple constant malfunctions;

- operational safety based on test-free fault localization, i.e. stopping work at the moment of failure of an element, which excludes the issuance of unreliable information, with simultaneous localization of the scene of the event:

- an increase in the number of suitable ranks due to the insensitivity of the scheme to the spread of parameters:

- uniformity of current consumption;

- simplified testing: functional tests are simultaneously checking for malfunctions;
- increased service life due to insensitivity to aging:
- ease of connecting schemes to each other due to the absence of forced synchronization:
- high efficiency of creating reliable products:
- ease of control and reservation,
- there is no problem of controlling the control schemes,
- a significantly smaller amount of hardware costs (not less than 1.5 times) with the same failure coverage ratio.

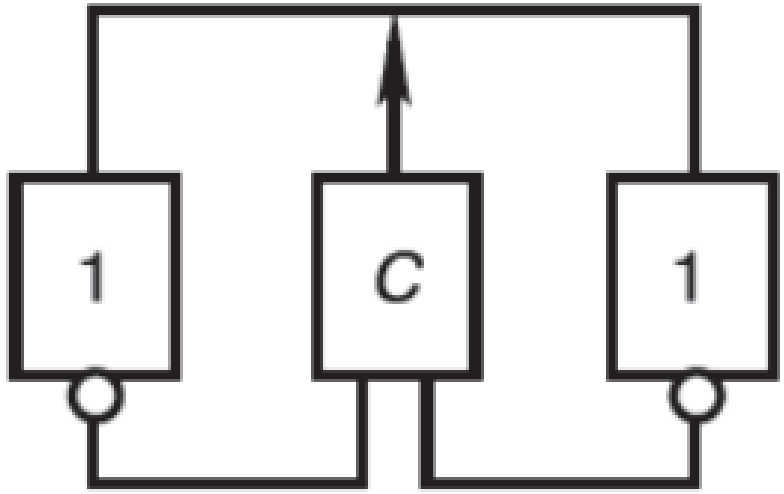
Reasons for the slow development of self-synchronous circuitry
1) the traditional focus of the manufacturing industry on synchronous circuits.
2) the unusual construction and operation of SS-schemes.
3) lack of experience in building SS-schemes and tested SS-solutions at the level of library elements.
4) lack of literature at the development level.
5) the development of SS circuit engineering in the field of special systems, which are out of sight of the developers of the shafts of universal systems.
6) large consumption of equipment or crystal area in comparison with synchronous systems for those applications where increased reliability of the equipment is not required.
7) the greater complexity of designing SS schemes and the complexity of developing CAD systems.

Theoretical foundations of self-synchronous circuits.

Unlike synchronous, as well as other types of asynchronous circuits, CC circuits can work with any delays of their elements. The delays of the elements will be considered arbitrary, of finite value. In these conditions, SS-schemes must be built in a special way.

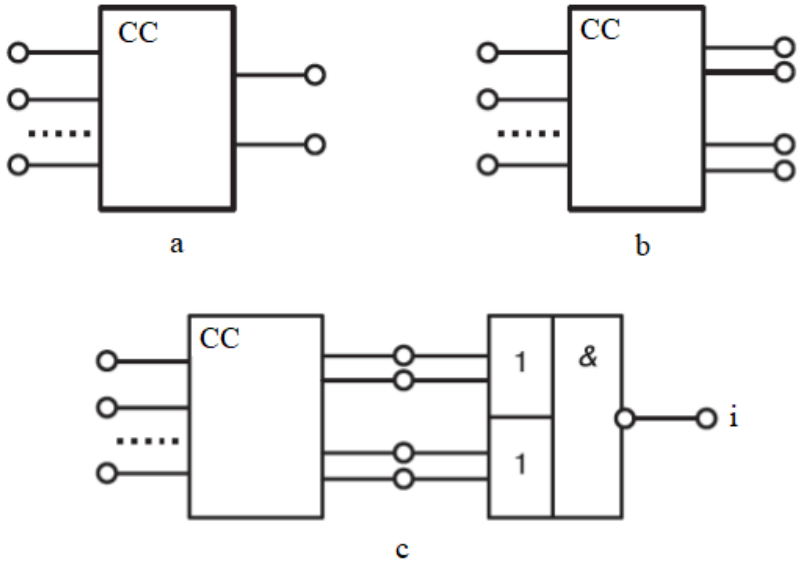
Principles of construction and operation of SS schemes

SS schemes can be built in different ways. In many theoretical works, diagrams illustrating the theory are given, but have no practical application.



Self-synchronous (speed-independent) circuit with Maler's C-element.

The diagram shows two parallel channels (process) of two inverters and a connecting Maler C-element. It is this element that allows you to connect two processes correctly, without races. However, Maler's theory provides only a tool for analyzing SS schemes. For their practical construction (synthesis), it is necessary to consider open schemes that have significant inputs and outputs for them. For example, let's take a scheme with two outputs.



Combination circuit (CC): a - output circuit; b - scheme in codes;
c - scheme in codes with an indicator; i - indicator signal.

Indication.

For the construction of any discrete circuit, it is fundamentally important to know the moments of the end of transient processes in various parts of the circuit or the delay of its elements. In synchronous circuits, this knowledge is taken into account a priori and determines the repetition period of clock signals.

To determine the moments of completion of transient processes at the outputs of the circuit means to generate some binary signal that reports the end of the transient process in response to a change in the inputs of the circuit. Such a signal will be called an indicator (I-signal) and the scheme of its formation - an indicator.

Code indication.

The two circuit outputs are independent of each other and can take the following combinations of values (let's call them their working sets): 00, 01, 10, 11.

Suppose that with some change in the inputs, the output signals should go from set 01 to set 10.

Such a transition can take place in the following ways:

01 → 10;

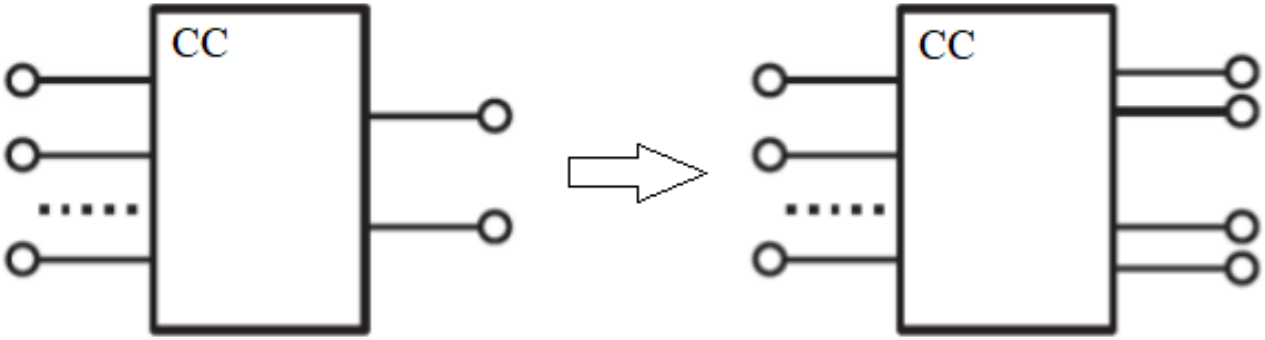
01→00→10;

01 → 11 → 10.

Whatever the transition path, any subsequent set after 01 is also working, and we have no way of knowing whether the transition has finished or is still in progress. Thus, in a "normal" scheme, with "normal" outputs, it is not possible to find a way to determine the end of transient processes.

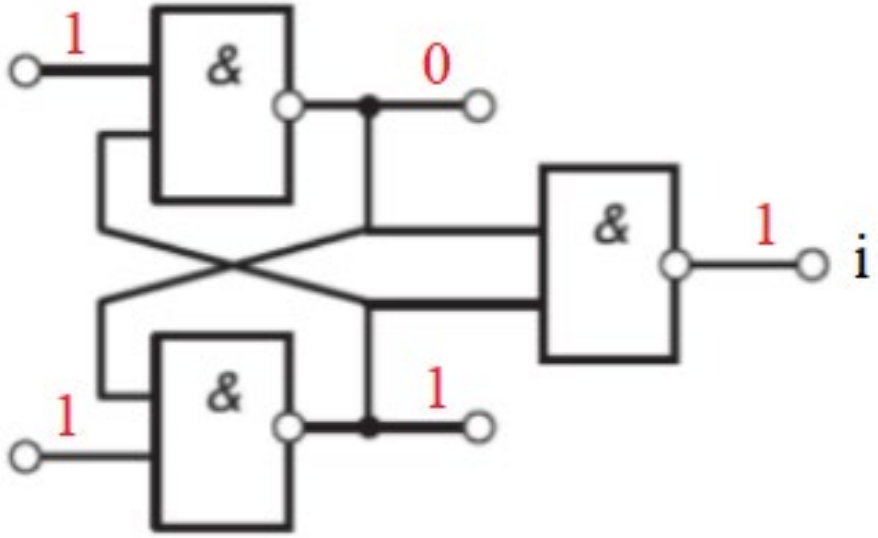
The only solution to this problem is the following: it is necessary to expand the code space of the output signals by including several transition sets in addition to the working ones. These sets must not overlap to be easily visible using simple electronic circuits. In other words, it is necessary to apply redundant coding of circuit signals.

Let's take the following encoding method:
an output value of 1 is coded as 10 and a value of 0 is coded as 01.
In this case, we go to the equivalent circuit.
For her, four sets will be working: 0101. 0110, 1001 and 1010, and the other twelve out of sixteen possible ones will be transitional.
Next, we will assume that all transitions between working sets occur only through transitional sets.



Under the accepted conditions, the transition 01 → 10 of the original scheme can be implemented in an equivalent scheme, for example, like this: 0110 → 0010 → 0011 → 0001 → 1001.

Two ideas of BC indication (Bistable cell).
The first idea is an indication using only BC.

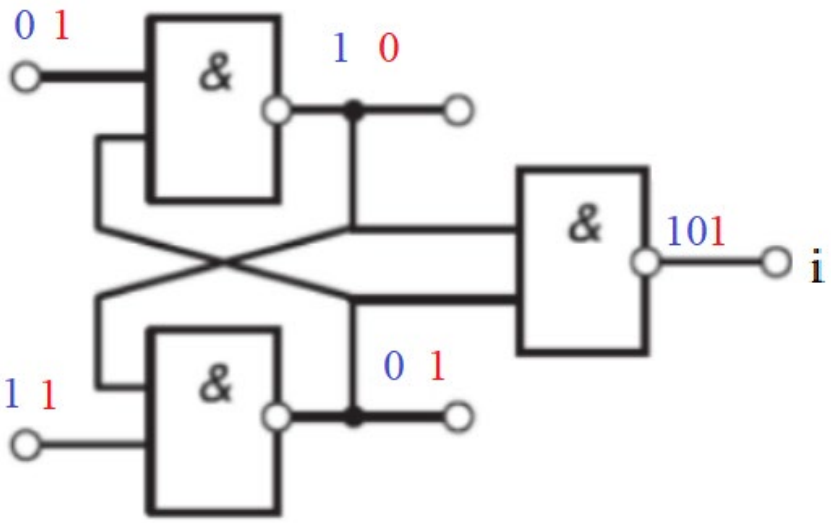


Suppose, in the initial state, the inputs of the cell have the value 11, the outputs - 01, the indication signal -1 (see the figure above).

Let's apply the value 01 to the inputs.

Then the outputs will change as follows: 01 → 11 → 10, and the I-signal 1 → 0 → 1, respectively.

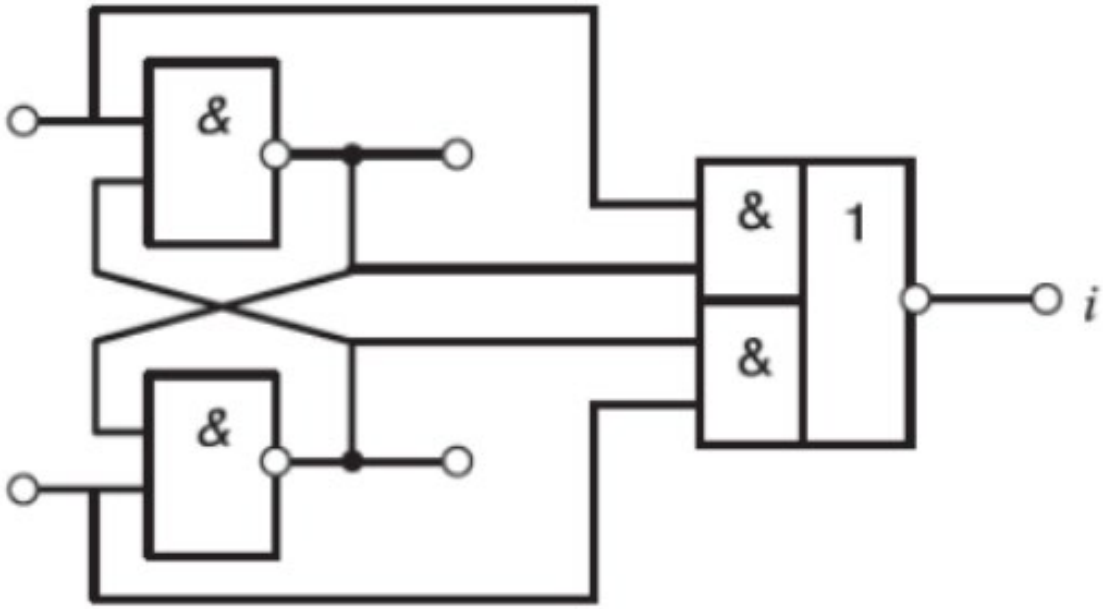
Thus, the value "1" of the signal shows a stable state of the BC, and "0" - a transient one.



However, to use the indication in SS circuits, it is necessary to match the cell inputs and the indicator output with the operating phase. For BC, this means that the i-signal in the case of identical cell inputs must differ from its value in the case of opposite input values.

For this method of indication, matching is achieved only in the extinguishing mode (in the figure, the inputs must be equal to 00). But in this mode, the information previously recorded in the BC is destroyed. For this reason, the first idea was not used in SS schemes.

The second idea involves memorizing information and matching phases.



It consists in establishing the fact of correspondence between the inputs and outputs of the BC. If the outputs correspond to the inputs, then the transient processes have ended, otherwise - they are not completed. In the figure, the signal for this method changes as 0 → 1 → 0, where 0 is a stable state, 1 is a transient.

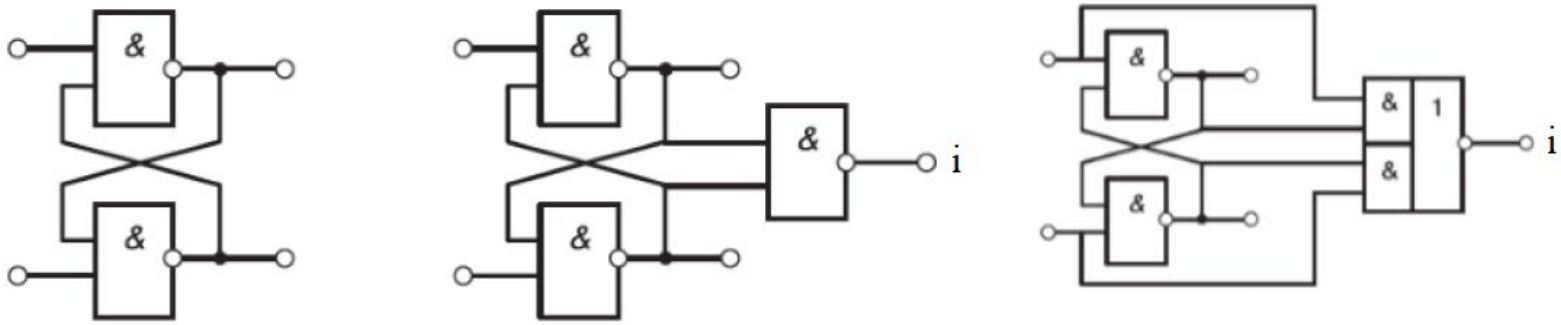
A fundamentally important point in both variants of the indication is that. that according to the construction, the output of the indicator element indicates the end of transient processes not only in the main circuit, but also in itself. In other words, there is no need to build a special display scheme for the indicator, which is not necessarily true for other approaches, such as physical.

Two-phase discipline.

Let's return to the combinational scheme of the figure.

Let its uncoded outputs still make the transition 01 → 10.

Due to the fact that the delays in the scheme are arbitrary, with a certain ratio of them, a collision may occur in the scheme in figure.



For example, output coded signals implement a transition:

0110→0010→1010→1011→1001.

In this case, the first pair has already completed its transition to the news state, and the second pair, due to longer delays, has not yet had time to change. As a result, state 1010 occurred in the middle of the transition, and the indicator should show the completion of the transition process, although in fact it is infinite.

In order to exclude such collisions, which give rise to signal competition, a requirement is imposed that the appearance of other working sets, except for the initial and final ones, is inadmissible during the transition, that is, there must be compliance with the discipline of transitions.

Experience has shown that the most effective and simple discipline is the following: among many transition sets, one or more special sets called spacers are distinguished. All signal transitions are subject to the requirement that they necessarily occur through spacers.

In this case, each transition is carried out in two stages (in two phases):

- from the initial working set through the intermediate ones to the spacer

- then from the spacer to the final working set.

Such a discipline was called two-phase.

The transition phase from the working set to the spacer is usually called the spacer phase, and from the spacer to the working set - the working phase. In the working phase, those functional signal transformations for which the scheme is intended (logical operations, summation, etc.) are implemented.

To simplify the indication as much as possible, it is advisable to choose spacer sets that are as easy to distinguish as possible! from workers Therefore, sets with the same values of connected code signals, for example 0000 or 1111, are usually taken as spacers.

Classification of self-synchronous circuits.

In the literature, the use of the term "self-timed" has a multifaceted nature and means only the use in specific digital products of one or another additional means of synchronizing the operation of the equipment in comparison with traditional methods. If we approach it formally, then the elements of using the SS approach are present in all commercial products of non-volatile memory that allow multiple recording of information by the user - RPSD (reprogrammable permanent storage devices; NRWM - nonvolatile read-write memory) - a specified mode of self-synchronous recording or self-synchronous programming mode.

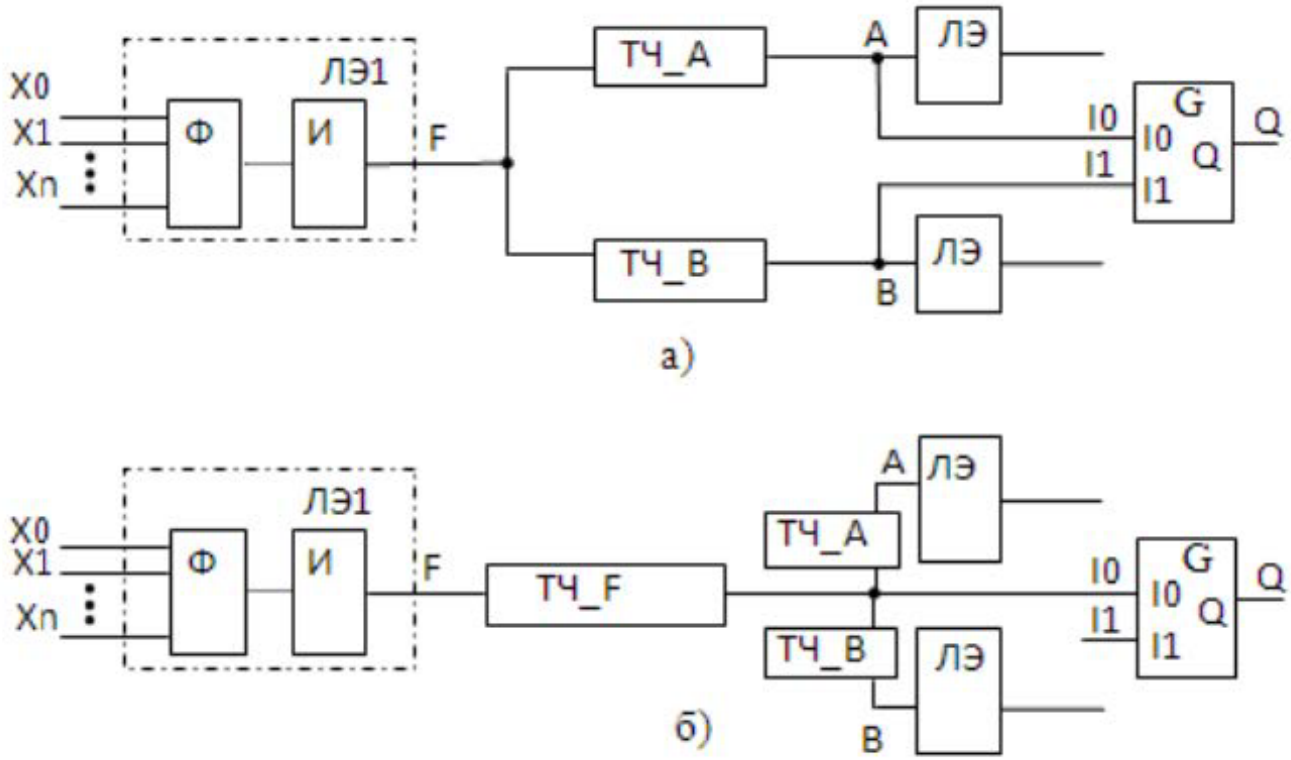
Four main groups of asynchronous circuits can be distinguished:

1) circuits that do not depend on speed (speed-independent, SI): delays of elements are arbitrary, but finite: the spread of delays in wires after branching does not exceed the minimum delay of the element;

2) circuits quasi-delay-insensitive (QDI): circuits that do not depend on delays of elements, on delays of isolated (long) wires and on delays in wires after branching, if they are not critical; can be designed within speed-independent schemes;

3) circuits insensitive to delays (delay-insensitive, DI): arbitrary but finite delays of elements and wires: such circuits give greater redundancy;

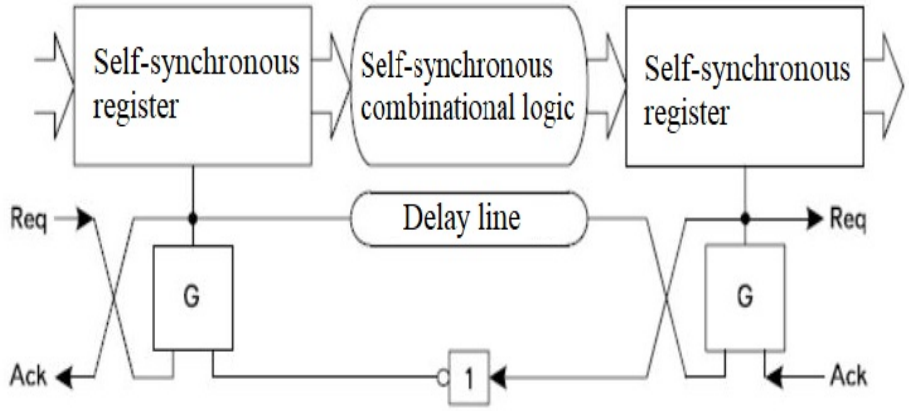
4) circuits with bounded delays (boundeddelays, BD): reasonable limitation of delays of elements and wires.



Two-wire and single-wire indication.

The most common method of constructing quasi-self-synchronous circuits is the maximum delay model method.

In these circuits, a combinational circuit model is used to form the signal of the end of the transient process, performed on a delay line, which corresponds to the maximum signal propagation time in the combinational circuit with some margin, which eliminates technological spread and errors in the estimation of the signal propagation time. This approach, in contrast to the synchronous circuit, enables the circuit to work at maximum speed under the given external conditions and parameters of the semiconductor structure.

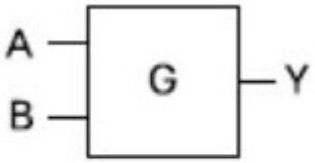


An example of a quasi-self-synchronous circuit is shown in Figure. Data between registers is transmitted using a special exchange protocol and is accompanied by request/confirmation signals (Req/Ack).

Construction of a quasi-self-synchronous circuit.

To synchronize the operation of the circuit, a delay block equal to the time of the critical path of the combination circuit and a set of G-triggers with additional NO elements are used.

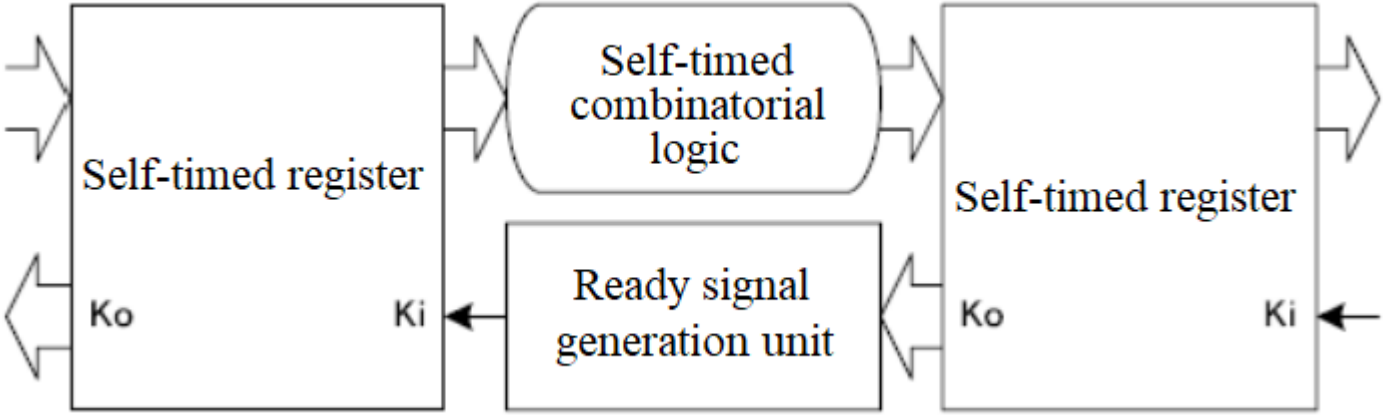
The G-trigger is a switching element with hysteresis, its switching occurs only when the same logic levels are present at its inputs. If the levels are different, then such an element retains its previous state. A conditional graphical representation of the G-trigger and its truth table are shown in figure.



$Y = AB+Y^{-1}(A+B)$

A	B	Y
0	0	0
0	1	storage
1	0	storage
1	1	1

In strictly self-synchronous schemes, direct determination of the moment of the end of the transient process is used. One of the ways to build such schemes is paraphasic presentation of signals. Two physical lines are used to transmit each bit of information. This makes it possible, in addition to two logical states, to transmit a separator separately, which allows you to separate the transmitted data in time and determine with its help the moment of the end of the transition process. When designing such schemes, additional requirements for monotonicity and the possibility of indicating at the output the end of all transient processes within the scheme are



imposed on the synthesis of the combinational function. The figure shows an example of such a scheme.

An example of the implementation of this approach is the NCL logic (NULL Convention Logic) developed by the specialists of Theseus Research, Inc. The class of strictly self-synchronous circuits has a number of advantages in comparison with synchronous and quasi-self-synchronous approaches.

These include:

- the maximum possible speed of the scheme, because the scheme itself determines the pace of its work depending on external conditions and processed data:

- independence of circuit performance from signal delays and logic elements,

- a wider operating range of the scheme, for the efficiency of the scheme only the preservation of the switching properties of the transistors is required:

Reduction of energy consumption due to the fact that in the absence of data in the circuit, signal switching does not occur and only static consumption remains, in contrast to the synchronous circuit, where without the use of special measures, regardless of the presence of data, the clock signal is applied to the triggers.